Replace the paragraph beginning at page 3, line 17 with the following paragraphs:

Further advantages, features and details of the present invention will be elucidated on the basis of the following description of a preferred embodiment thereof with reference to the annexed drawings, in which:

Fig. 1 is a functional diagram of a graphic application of the data processing circuit according to the present invention;

Replace the paragraph beginning at page 5, line 10 with the following paragraph:

The bus structure 26 (Fig. 3) comprises a control SC-bus 51, an A-bus 52, a B-bus 53, a Q-bus 54, an F -bus 55, an M-bus 56, a U-bus 57, a D-bus 58 and a V-bus 59, each of which is, for instance, 32 bits wide. Each of several functional units of data processing circuit 1 drives its own output bus and has a separate, dedicated output (bus) register/driver for its bus, which can be read in the following cycle by various other functional units. For example, multiplier 23 drives the M-bus 56 using its bus register, M-reg 66; ALU 31 drives the F-bus 55 using its bus register, F-reg 64; shift register 25 drives the Q-bus 54 using its bus register, Q-reg 62; register bank 33 drives the A-bus 52 and B-bus using bus registers, A-reg 60 and B-reg 61, respectively; image input and output circuitry 30 drives the V-bus using its bus register, V-reg; and so forth. This approach allows parallel processing for all of the functional units.

Replace the paragraph beginning at page 5, line ~~13~~ 13 with the following paragraph:

The register bank 33 is connected via output registers 60 and 61 to the A-bus and B-bus, respectively. A register bank 33 contains ninety-six inputs which are single 32

bit, double 16 bit or quadruple 8 bit words. Three ports enable simultaneous performance of two read actions and a write action. Sixty-two of the ninety-six registers are directly accessible. The remaining thirty-two inputs are addressed via the vector index generator 32 which can generate a maximum of 12 locations per cycle (i.e., four byte sections for each of the three ports, since each word segment can be selected separately within the registers).

Replace the paragraph beginning at page 5, line 21 with the following paragraph:

The parallel shift register 25 is designed such that it can shift 32 bits of data anywhere from 1 to 32 positions to the left or right in one clock cycle based on the information received via the A-bus 52. The information can be grouped into one, two or four sections of 32, 16 and 8 bits respectively. The shift can take place logically (unsigned), numerically (unsigned) and rotatingly. The operations are received from the B-bus 54 or the F-bus 55. The parallel shift register 25 is connected via a register 62 to the Q-bus 54. Fig. 8 schematically shows an example of the two step rotation of a 32 bit word (consisting of two 16-bit bytes) through 11 bits in a positive direction by way of four 8 bit rotations and eight 4 bit crossings.

Replace the paragraph beginning at page 6, line 2 with the following paragraph:

With reference to Fig. 3, the arithmetic logic unit 31 (ALU) is connected to the A-bus 52, the Q-bus 54, the M-bus 56, the D-bus 58, the U-bus 57, the B-bus 53, the F-bus 55, again to the U-bus 57 and the V-bus 59. All the usual logic operations of a conventional ALU can be performed by the ALU 31 of the present invention in addition to numerical functions such as addition, subtraction, increment and decrement. The ALU 31 is further provided with a so-called parametric logic function. On the basis of the content of an 8 bit register, the ALU 31 can perform a random combination of 256 possible logic operations on 3 operands. The standards for X-window and MS-

Windows specify that logic and graphic operations must be possible in any combination. The parametric function can also be used to realize shifting, masking, combining or comparing operations in a single clock cycle.

Replace the paragraph beginning at page 8, line 10 with the following paragraph:

The drive of the image memory 29 is adapted to generate an address on the basis of the X/Y position so that any random image segment can be addressed on the basis of its location and the image in the image memory. The image memory is also suitable for storing other databanks such as lists and databanks with graphic elements.

Replace the paragraph beginning at page 8, line 13 with the following paragraph:

The data processing circuit 1 can be programmed in a higher program language, such as C, so that it is easily programmed, as in RISC and CISC processing units. The data processing circuit 1 can be programmed with instructions according to the RISC concept as well as with the CISC instructions of a personal computer. In order to achieve a large increase in speed for graphic applications, the programmer can program all functions of data processing circuit 1 at a lower-level via an instruction field of 64-bits. The ALU 31 and the multiplier unit can be set to parallel operations, whereby the speed for graphic applications can be increased by a factor of 4-20 as compared to existing RISC processors. For a particular application, a programmer will set a "once-only" series of instructions and control registers. Subsequently the programmer will start the processor with one command, hereafter the processor independently processes the pixel flows.

Replace the paragraph beginning at page 9, line 21 with the following paragraph: